NetSeminar Q&A for Effective Ways of Testing BER on 40 Gbps High-Speed Interface Devices (Nov. 6, 2001)

The following questions pertain to the Agilent 40G Industry Buzz.

Q: In your opinion when will 40G become realistic?
A: My own (Larry DesJardin) observations here are that we are in the middle of field trials now of 40G long haul equipment. I think several of these have been noted at the OFC conference and so forth. My guess of what's going to happen is that there will be numerous field trials through the year 2002, of service providers really trying to test out some of the long haul equipment and other equipment being developed. You are probably going to see the first commercial deployment in 2003. That's where I think you will really have things being deployed, not necessarily in high volume. And then I believe it's really going to be when is that crossover point where 40G is more cost effective than 10G where you really see the high volume. My guess is sometime in, let's say, second half of 2003 you would probably see that occur.

Q: Do you think the RBOCs will move to the 40G model?
A: Quite frankly, it's really more of the long haul applications, which are more likely to use the 40G technology initially, than the shorter haul applications that many of the RBOCs have. I think long-haul services using 40G will occur at the end of 2003. I would expect to see more RBOCs looking seriously at 40G in perhaps 2004, but again I will put an asterisk here that I could be wrong. What I have seen in the industry is basically different segments of the market being attacked by different 40G equipment suppliers. So my prediction above could be reversed.

Q: What is the wavelength range of the 83453A High Resolution Spectrometer (HRS)?
A: The HRS wavelength range is 1510 nm to 1640 nm. However the mode hop free range is 1520 nm to 1620 nm.

Q: What's the optical bandwidth of the 83453A High Resolution Spectrometer (HRS)?
A: We have three resolution bandwidth settings: HighRes, Normal, and Wide. In the HighRes Mode the best achievable resolution is 1 MHz. In Normal Mode the best achievable resolution is 18 MHz. In Wide Mode the best achievable resolution is 200 MHz. The optical bandwidth of the 83453A is around 18 MHz.

Q: How do you define long haul? How long is long?
A: Our definition of long haul is several spans, each one of which is probably between 60 and 100 km. The kind of things we're hearing in the industry for 40G might be anywhere from 60 to 100 km per span, and doing perhaps five span of those now, and perhaps ten in the future. So anywhere from 300 to 1000 km would be a long haul. This is to be compared against metro, which might be a very short single span of 40 to 80 km or so, and also to be differentiated from submarine and ultra long haul, that could be thousands of kilometers.

Q: Where do you think the main impact of 40 Gbps will be felt?
A: My guess (Larry DesJardin), and there are a lot of different opinions on this, is in the core part of the network, both in long haul transmission in the core, as well as the equivalent routers and switches that would be interfacing with that equipment. I think the first applications are in the core, and first real deployments in 2003.

Q: Does Agilent have any test methodology or solutions that can provide solutions for both AC and DC parametrics?
A: In general, yes. The combination of the bit error rate testers and our DCAs you can do a lot of analysis both in the DC and AC domain, particularly when these are put together.

The following questions pertain toward BER Testing.

Q: Is there a standard pulse shape for RZ encoding?
A: Basically no. There are many pulse shapes that various companies are interested in using, but those are all proprietary schemes for creating that RZ pulse. RZ pulses are used exclusively in long haul and ultra long haul

applications where both ends of a system are composed of equipment from a single supplier, so there has not been a big move to standardize RZ pulse shapes between manufacturers. Some people are very interested in what are called solitons, pulse shapes that preserve shape and maintain timing over a long distance. Doing so requires generating a very exotic type of pulse shape along with phase modulation. In general, there are so many different schemes that we can't really call one a standard.

Q: Please define Chirp.
A: Chirp is defined as frequency modulation (or wavelength shifting) during pulse transmission. The term originated from the wireless Morse code days when this frequency shift was audibly heard as "chirp". It is a side effect of many amplitude modulation techniques. Therefore, chirp is essentially an unwanted modulation characteristic that results from many types of transmission techniques. Often a side effect of the various transmission techniques used is that some additional phase modulation is created in the process. For example, with current modulation of a laser diode, which is a technique that's been used for a long time in the CATV industry, the change in the current that's driving the laser diode results in changes in the material properties of the active region of the laser, and that essentially causes the frequency of the laser output to change slightly. So if you think about how frequency modulation is related to phase modulation, in this attempt to change the power level of the laser one gets some additional phase modulation that wasn't intended. The problem with chirp for long haul networks is that it broadens the total spectrum taken by the signal, and different frequencies travel at different rates of speed over a long length of fiber As a result, the timing characteristics of those different spectral components can get out of whack and essentially interfere with each other. This is particularly true for 40G, where a delay of 25 ps has delayed a signal component from one transmitted bit to the next.

Q: You indicate that the complexity of silicon is high compared to the compound semiconductors. Can you explain what you mean by complexity?
A: Obviously silicon is easier to grow than some compound semiconductors (SiGe, GaAs, InP). It's something that the electronics industry has been doing for a very long time. What we mean by complexity is that the additional circuitry required to clean up the timing associated with these high-speed data waveforms results in an overall more complex circuit when we try to implement clock recovery circuits and so forth in silicon. It results in more overall circuit complexity than if we use some of the other materials that are inherently faster.

Q: What lab or field trials has Agilent has actually done in terms of developing a 40 Gbps tester?
A: Agilent labs has for close to a year now been working with essentially a bench top set-up actually creating 40 Gbps RZ streams as well as measuring the BERs associated with those streams. And essentially we are moving that bench top set-up into production as we speak.

Q: What types of post-processing of acquired data have you found customers doing? And how is this connectivity to a computer platform accomplished?
A: We know that some customers have been interested in doing post-processing with recirculating loops, which does require typically some type of post-processing of the data because it's very difficult to get the hardware in time exactly to capture all the necessary data. For post-processing some of the data what we have seen are a lot of applications where people are looking at BER sensitivity to some sort of factor. The bathtub curve is something a lot of people are looking at. Bit error rate versus power level is another one that we have seen people use. And so a lot of times it's BER versus some other system parameter that they are trying to quantify.

Q: How is BER determined when PRBS has to be encapsulated within a packet?
A: A lot of times there are two different methods, depending on the type of BERT you have. One of them if it's a memory type device, the pseudo-random pattern will be in the packet and the header information will be at the front end of the packet, and you just compare both the header as well as the PRBS pattern. On BERTs that generate a SONET frame, the analyzer side will also be comparing to the complementary analyzer pattern. The thing that has to be taken care of, there are certain key control lines in the overhead byte, such as the B1 byte, which change dynamically. There are tricks with memory-based testers to address this. Functional testers, with hardware algorithms, can do this automatically.

Q: Are there other graphical representations that are meaningful to engineers besides the eye?
A: Certainly people are interested in looking at the waveforms directly in time, although that is very difficult. Part of the difficulty is for instance the optical sampling architecture that we mentioned really only works for

repetitive waveforms as opposed to truly random sequences. There are other types of measurements that can be done, spectral measurements on these types of signals that can be very meaningful. Also, BER vs. time within a pulse period, commonly known as the bathtub curve, is very common.

Q: Did you say future BER testers will have differential data inputs?
A: I think as systems develop, because so many multiplexers and demultiplexers devices have differential input or outputs, it's becoming common to see high speed BERTs have high differential data inputs. Just because a BERT has a differential input, a properly designed BERT will not necessarily require you to use a differential input but it will be available if the particular device you are testing can use that. Also, optical data inputs are important to many applications.

Q: Can you imagine a creative 3D graphical representation of BER that would be meaningful?
A: Yes. We have played around with some post-processing of data using a mathematical package called MATLAB, to create a 3D bathtub measurement which covers both the sampling point versus the amplitude point and creating a 3D pattern. That's been done by some people using third party software packages. Any measurement of BER vs. two variables would be a good candidate.

Q: Does differential signal reduce the bandwidth available for signals?
A: In general, it probably should. The specific answer depends a lot on specifically how the differential input or output is implemented in hardware. It depends a lot on the types of devices used.

Q: Has there been much thought to date regarding physical connection of these devices to ATE for production test?
A: Some of it has been discussed. The common type of elements, especially for the electrical contacts, is what's called a 1.85 mm connector. They are somewhat sensitive in terms of robustness, but currently does offer a 65 GHz bandwidth. On the optical side, there is essentially no difference on the connectivity based on data rates, and there are note the signal integrity issues versus length that there are for electrical signals.. So on the optical side nothing has changed, but on the electrical side the connectors are becoming more critical in terms of space.

Q: When testing with long PRBS or SONET scrambled data there are deterministic events that occur on random time frames. How do you deal with that?
A: This is a good application for a dedicated OC-768/STM-256 functional tester. Hardware algorithms will create and compare the patterns.

Q: Has anyone achieved 40 Gbps transmission with a NRZ type transmission?
A; Yes. In particular, it appears what's common operating practice out in the world is that all short reach and intermediate reach signals (that might be between clients like a SONET add/drop muxes, routers and so forth, to DWDM equipment on the client side) will in fact be NRZ. The standard STM-256 or OC-768 signal will be NRZ. However when you go to the long haul side of the network, which is a proprietary interconnect only between a single vendor over long distance, that typically has been RZ. I do know of experiments being done on what can be done with NRZ in that space, but generally there are RZ modulated signals on the long haul side.

Q: If the system under test has long delay, is there any trick to synchronize the data from the system to the expected pattern?
A: When you use the word trick, I tend to think that there are no methods that you can use that don't involve having some kind of timing reference. If you are talking about a pseudo-random bit stream, the difficulty is that in order to use some type of trick you would need to have something that you can measure that changes as a function of the delay. And the problem with a truly random sequence is you only get a good bit error rate when you are exactly in time, so there aren't any tricks that I know of unless your pattern isn't fairly random.

Q: What is the feasibility of testing BER jitter in wafers for SONET devices and what do you take into consideration under that scenario?
A: Typically if you take a look at the kind of devices like multiplexers, demuxes and so forth, even if they are eventually used in a SONET application, the common practice is to use standard PRBS sequences and so forth. Not a specific SONET pattern. The only things which are really SONET specific end up being framer chips and

so forth, which typically are tested at certain parts by using parallel word sequences or by using something let's say totally memory based IC type test of input and output sectors and masking and so forth. Some of our products, like the ParBERT, can do that. If there is a desire to test the device with an actual SONET pattern, then a pattern can be downloaded into ParBERT memory that is PRBS embedded within SONET. So, instead of using the hardware PRBS generators within ParBERT, a specific pattern is downloaded and repeated over and over.

Q: I have used noise loaded measurements to determine the slope sensitivity of a receiver to reduce the measurement time. How do I know there isn't a low rate error floor? I would run a one-hour bit error rate test to look for error floors, but this takes too much time. Do you have any suggestions for testing for error floors?

A: There is a multi-part answer to this question. One of the ways that we know there isn't a low rate error floor is because the statistics associated with the noise tends to be Gaussian. Therefore the expected measurements are very predictable and that's one reason most people find that type of slope sensitivity measurement useful in terms of predicting what the measurement floor will be at a lower bit error rate.

One approach that a lot of customers have taken who are interested in reducing their test times for lower data rates is what they call Q factor measurements. Essentially Q for quality. Slide 22, titled "When Good Bits Go Bad", shows the two curves associated with the noise. A lot of customers have taken the approach of arbitrarily moving the decision threshold around and measuring the bit error rate for each setting of the decision threshold in order to see how that signal to noise varies. Essentially they use a more mathematical approach to calculating what the noise is under certain conditions.

The final part of the answer is as you go to higher data rates the test times automatically reduce so the kind of problem you are talking about may not be a problem for you.

Q: What would you suggest for production BER testing where a long duration test is not tolerable?

A: As opposed to doing a long duration test you can do a slope sensitivity measurement, where you arbitrarily add noise, measure the BER at different noise levels and extrapolate on a curve what the minimum BER is. That will reduce test time.

Q: Why is using D and D bar seem to be totally uncorrelated?

A: While you are using D and D bar, that can be uncorrelated, you are correct. They are uncorrelated but it is not correct to say totally. This is a maximum cheapest way we can get the two signals going through the two various modulators as uncorrelated as possible.

Q: Is synchronization the hardest challenge for 40 Gbit testing?

A: Yes and no. It certainly is one of the hardest challenges associated with building this type of measurement system. But the other challenge is getting what is frankly state-of-the-art technology like some of these modulator type devices, etc.

Q: In testing 40 Gbps data streams doesn't the hardware limit the number of signal harmonics passing through the system, thereby making the output less square and subsequently affecting the decision region in the eye and the observed bit error rate?

A: Yes. When we use the term "square" at 40 Gbps, we should probably be using triple quotes or quadruple quotes.

Q: What kind of penalty do you think will be introduced by D and D bar methods?

A: Currently we have not seen, in talking to various customers, any penalty in doing that. Obviously your test times will increase because now you are only able to analyze one channel at a time. But with the price of the current equipment that's available, it's probably the best method of doing it right now.

Q: The SONET header contains a set sequence of 768 bytes of hex f628. Will that present a problem at 40 Gbps?

A: I will describe what I see the critical part of this question. Basically what's happening here is every time the SONET header is sent, which is every 125 microseconds, there is going to be this set pattern. What that means is the spectrum that is sent is technically slightly different from your robust PRBS sequence and so forth. If people are interested in testing devices that will be used in SONET equipment but are not requiring a SONET pattern, such as a mux/demux CD-R CRC and so forth, I think the industry standard practice for testing those still is using a PRBS is the most robust test you have. However, if you really want to be sure about this, what you can do is basically if your BERT is capable of having pattern memory in it, which our 40G BERTs are capable of, is basically loading in the SONET header PRBS data in the payload and you will then get the right spectral response there and you can use that to test. A lot of times that may be done in R&D to make sure your clock recovery circuit doesn't have something funny going on. Typically, though, in your standard wafer test you will run standard PRBS.

Q: What is the maximum cable length you can use to connect the electrical I/O of the BERT to the test equipment?
A: It's very dependent on what you are trying to test. As illustrated in one of the slides, a 24-inch cable at 40 Gbps can have up to 7 dB of loss. If that loss is too excessive based on two things, one is voltage level that needs and two, what the maximum output voltage of your tester is. Those things need to be taken into consideration. Obviously at this data rate the shorter the cable the better, your rise and fall time start degrading over time, over length of cable. We have used 24-inch cables without any degradation except for signal loss.

Q: What type of FEC is typical for OC-768 and higher transmission rates?
A: The first is RS, which is Reed Solomon, is the prevalent code. In particular what I think is going to occur in the long term is G.709 standard, which is going to have a specific Reed Solomon code at a rate of 255 over 236, which is about an 8 percent overhead.

Q: Is there any suggestion to compensate mismatch loss and noise caused by test probes during a wafer sort test at these 40G data rates?
A: There isn't a specific answer to this question. Probing devices is something that is a common problem that has been attacked by people, for instance, using very high-speed network analyzers. I would say to look to some of those folks. They have dealt with a lot of same problems for high-speed network analysis. For things like differential termination and impedance matching, it would probably end up being a custom circuit design solution for the case that you are talking about.

Q: Do you see jitter testing at 40 Gbps being done in the manner of FibreChannel and Ethernet or more like SONET with jitter tolerance transfer generation?
A: It's going to be the latter. 40G is OC-768, which is a SONET standard. Everything I can see in the industry is to basically take the OC-192 standard and multiply it up by 4 and maybe tweak it a bit, so it's going to have more of the tolerance transferred generation standards you see in SONET.

Q: Do you know if there are companies testing full speed at wafer sort on 10G SONET devices? Is this really possible? And also for 40 Gbps devices?
A: Yes. Currently some people are doing at speed wafer testing at 10G, and are looking at doing the same at 40G. Others do a low speed functional test, and then test the device at full speed once it is packaged.

Q: Does Agilent plan on making E/O and O/E converters at 43.2G?
A: The answer is we are doing more than planning it. We are incorporating those types of devices into our current 40 Gbps BER testing solution. If you are asking if they will be available as separate components, they probably will be but the timing of that is not clear yet.

Q: Why does the industry persist in using NRZ transmission that makes the transmission a lot more susceptible to jitter because of clock recovery issues?
A: I think the bottom line IS the bottom line, it's due to cost. I think what people are looking at is seeing if they can make a very low cost modulator for short reach type signals. And this might be using electro-absorption modulators or some way of turning on and off the laser where the chirp is not a critical factor. The alternative is if you go to RZ you typically are running at least two Mach-Zehnder modulators, each very expensive, some additional clock recovery circuits, very expensive, and it doesn't look like that kind of performance is needed short reach. That's why everyone is looking at NRZ type modulation for client signals.

Q: Has CDMA ever been used in 40 GHz systems?

A: Several different kinds of coding technique have been used in trial basis. I think there are two complete sessions at OFC 2002 about using different kinds of coding techniques at higher rates. Everything that I see as a practical system deployment at 40G today is really using standard NRZ, RZ or maybe some sort of carrier suppressed variant of that.

Q: Is there an optical mux available or is this only an electrical method?
A: Currently at 40G the traditional method is using electrical multiplexers. What the future looks more and more likely is we move, believe it or not, to 80 and 160 Gbps on a system, at that point probably the multiplexers will start to become optical mainly because of the bandwidth limitations of your silicon or germanium, it's just not there. So currently at 40G it's pretty much electrical only. But as we move up to 160G and higher it will probably go to optical multiplexers.